10841/N

M-72/2110

COMPUTER ORGANIZATION AND ARCHITECTURE -113

SEMESTER- I, (Dec. 2019)

TIME ALLOWED 3 Hrs MM 70

NOTE: **The candidates are required to attempt two questions each from Section A & B Section C will be compulsory.**

Section A

Q1 Discuss the instruction cycle of a basic computer with a neat diagram. (10.5)

Q2 Design Full adder using NAND gates only. (10.5)

Q3 Design Decade counter. (10.5)

Q4 Define bit, byte and word. Discuss various number system used in the computer system. (10.5)

Section B

Q5. Design a four-bit combinational shifter to perform shift micro-operations. (10.5)

Q6. What is a Control unit? Compare RISC architecture with CISC architectures. (10.5)

Q7. Discuss the DMA controller in detail. (10.5)

Q8. What is mapping in the context of cache memory? Explain three types of mapping procedures used in cache memory. (10.5)

Section C

Q9.

I. Define control memory and microinstruction?

II. Distinguish between isolated and memory-mapped I/O.

III. What is the use of EEPROM?

IV. What is Virtual memory?

V. What are addressing modes?

VI. Why NAND gate is called a universal gate?

VII. What are the ASCII codes? How these are different from EBCDIC codes. 7 X 4 = 28